CLAIMS

WHAT IS CLAIMED IS:

1. A method to produce a memory chip, comprising:

presenting a memory substrate having a system region; and

fabricating a data cell region on the memory substrate.

2. The method of claim 1, wherein the date region defines an area and the system region defines an area that is substantially the same the area of the data region.

3. The method of claim 1, wherein the memory substrate further includes a word line pad and a bit line pad, each disposed about the system region, and includes an external pad disposed about the word line pad and the bit line pad, wherein the word line pad is coupled to the plurality of word lines and the bit line pad is coupled to the plurality of bit lines.

4. The method of claim 3, wherein the system region includes

a row address buffer coupled to an external pad and a row address decoder coupled between the row address buffer and a word line pad,

a column address buffer coupled to the external pad and a column address decoder coupled between the column address buffer and the bit line pad,

a sense amplifier coupled between the column address buffer and the bit line pad, and

an output circuit coupled to the external pad and the sense amplifier.

5. The method of claim 4, wherein the system region further includes an input circuit coupled to the external pad, the sense amplifier, and the output circuit.

6. The method of claim 1, wherein fabricating a data cell region on the memory substrate includes

forming a first stack having a first resin,

stamping the first resin,

etching the first resin to form a plurality of adjacent first stacks,

disposing a plurality of insulating layers between the plurality of adjacent first stacks,

forming a second stack on each adjacent first stack, the second stack having a second resin,

stamping the second resin, and

etching the second resin to form a plurality of adjacent second stacks.

7. The method of claim 6, wherein forming a first stack having a first resin includes forming the first stack on the memory substrate in the following order: a metal layer on the memory substrate and a silicon layer on the metal layer.

8. The method of claim 7, wherein forming a first stack having a first resin further includes coating the silicon layer with the resin.

9. The method of claim 7, wherein the first stack further includes a recording film disposed on the silicon layer.

10. The method of claim 9, wherein forming a first stack having a first resin further includes coating the recording film with the resin.

11. The method of claim 6, wherein stamping the first resin includes

placing the first resin under compression with a face of a first stamper, wherein the first stamper face includes a plurality of protruded and recessed areas, and

hardening the first resin while the first resin is under compression.

12. The method of claim 11, subsequent to stamping the first resin, fabricating a data cell region on the memory substrate includes removing the first stamper from the resin.

13. The method of claim 6, wherein each of the plurality of adjacent first stacks includes a word line and a data cell.

14. The method of claim 13, wherein each data cell includes a diode and a recording layer.

15. The method of claim 6, wherein forming a second stack on each adjacent first stack includes forming a metal layer on each adjacent first stack.

16. The method of claim 15, wherein stamping the second resin includes

placing the second resin under compression with a face of a second stamper, wherein the second stamper face includes a plurality of protruded and recessed areas, and

hardening the second resin while the second resin is under compression.

17. The method of claim 16, subsequent to stamping the second resin, fabricating a data cell region on the memory substrate includes removing the second stamper from the resin.

18. The method of claim 6, wherein etching the second resin to form a plurality of adjacent second stacks includes forming a plurality of adjacent bit lines at an orientation that is orthogonal to a word line.

19. The method of claim 18, wherein fabricating a data cell region on the memory substrate further includes disposing a plurality of insulating layers between adjacent bit lines.

20. The method of claim 19, wherein fabricating a data cell region on the memory substrate further includes forming a protection layer on the plurality of adjacent bit lines.

21. The method of claim 1, wherein fabricating a data cell region on the memory substrate includes

presenting a data cell substrate having a plurality of protruded and recessed areas,

forming a plurality of first stacks on the plurality of protruded and recessed areas,

disposing a plurality of insulating layers between the plurality of adjacent first stacks, and

forming a second stack on each adjacent first stack.

22. The method of claim 61, wherein the data cell substrate defines a data cell substrate axis that is normal to a plane of the data cell substrate and wherein forming a plurality of first stacks includes depositing at least one of a metal layer, a silicon layer, and a recording film onto the data cell substrate at an angle to the data cell substrate axis.

23. The method of claim 22, wherein depositing at an angle to the data cell substrate axis includes depositing from an upper diagonal direction.

24. The method of claim 22, wherein depositing at an angle to the data cell substrate axis includes depositing from an angle that is parallel to the data cell substrate axis.

25. The method of claim 22, wherein depositing at an angle to the data cell substrate axis includes depositing from a first angle and depositing from a second angle.

26. The method of claim 25, wherein depositing at an angle to the data cell substrate axis includes depositing at a first angle and depositing at a second angle.

27. The method of claim 25, wherein depositing at a first angle includes depositing from a first upper diagonal direction and wherein depositing at a second angle includes depositing from a second upper diagonal direction that is different from the first upper diagonal direction.

28. The method of claim 25, wherein one of the first angle and the second angle is parallel to the data cell substrate axis.